Low-Cost Single-Phase Powered Induction Machine Drive for Residential Applications

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Abstract— **In conjunction with the 2003 Future Energy Challenge (FEC), a low-cost integrated machine and drive system is considered for residential applications between 50 and 500 W. The objective is to remain cost competitive with traditional single phase induction machine solutions while improving system performance. The basic architecture includes a power factor correction boost rectifier, a hex-bridge inverter, control circuitry implementing selective harmonic elimination, auxiliary power supplies, and a three phase induction machine designed for inverter operation. This paper discusses system design, performance, cost, and lifetime.**

Keywords-induction motor; harmonic elimination; power factor correction; efficiency; low cost; single phase

I. INTRODUCTION

Currently, there exist approximately 1 billion motors in the U.S, which account for about 64% of the electrical energy used or roughly 1700 billion kWh/yr. Ninety percent of the motors are less than 1 hp in size, and account for approximately 10% of the electricity consumed by the electric motor population [1]. These fractional horsepower motors are primarily single-phase induction motors used primarily due to their low production cost despite their poor efficiency. A mere 1% improvement of efficiency in fractional horsepower market translates to 1.7 billion kWh/yr of energy saved [1]. These statistics are the motivating factors for the 2003 Future Energy Challenge (FEC) motor and drive system criteria:

Output power	50W - 500W (<1hp)
Motor Speed	1500 rpm (base, 10:1 load range), 150 – 5000 rpm (adjustable)
Efficiency	> 70%
Power Factor	> 0.80
Voltage Source	$120V_{ac}$, 60 Hz
Cost	$40 (million units/year)
Lifetime	10 years

The design objective was to minimize system cost while meeting aggressive performance specifications. The proposed system (named iDRIVE) consists of five subsystems: input power factor correction (PFC) boost rectifier, flyback converter, hex bridge inverter, controls, and a three-phase induction motor as shown in Figure 1. A relatively standard topology was implemented due its established reliability. One of the innovative aspects of the iDRIVE that allowed for significant efficiency improvements included implementation of selective harmonic elimination (S.H.E.) to reduce switching losses compared to traditional PWM techniques. Additionally, an induction motor was designed to optimize efficiency and performance when operated with an inverter as opposed to traditional designs, which make comprises to deal with line starting conditions.

The following sections present system design considerations and performance for each of the subsystems shown in Figure 1. Results of system lifetime and cost analyses are also presented in the paper.

II. PFC BOOST RECTIFIER

The requirement that the power factor be greater than 0.8 across all operating points necessitates power factor correction (PFC). A passive PFC solution was desirable due to the low cost objective of the project; however, simulations indicated that a classical rectifier provided a maximum power factor of 0.8 and power factors less than 0.7 were observed in hardware. These simulation results were confirmed in [2]. As a result of these initial tests an active rectifier was deemed necessary. An active boost rectifier [3] was chosen due to the wide availability of low cost control chips [4]. A nominal dc bus voltage of 200 V was chosen to maximize the PFC efficiency. This voltage also allowed less expensive lower voltage rating switches (400 V) to be used compared to typical drive bus voltages of 300-400 V.

The PFC boost rectifier was designed based on the Texas Instruments UC3817A IC and is shown in Figure 2. The capacitors are undesirably large, but are properly sized fo both voltage ripple and internal power dissipation (current ripple,

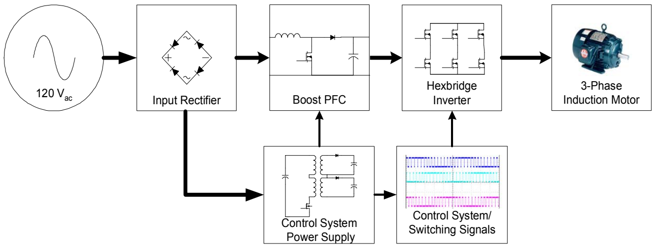

Figure 1. iDRIVE System Architecture Overview

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ESR). Inrush current was limited by an NTC thermistor. The voltage and current waveforms are shown in Figure 3 with an 800 W load. Figure 4 shows the measured PFC efficiency across the desired load range. The power factor was greater than .945 for input power greater than 50 W.

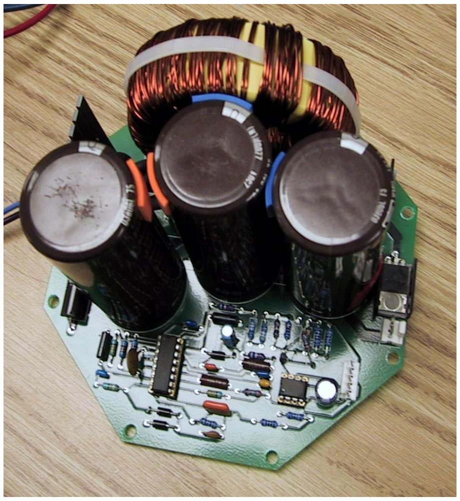

Figure 2. iDRIVE Active PFC Boost Circuit

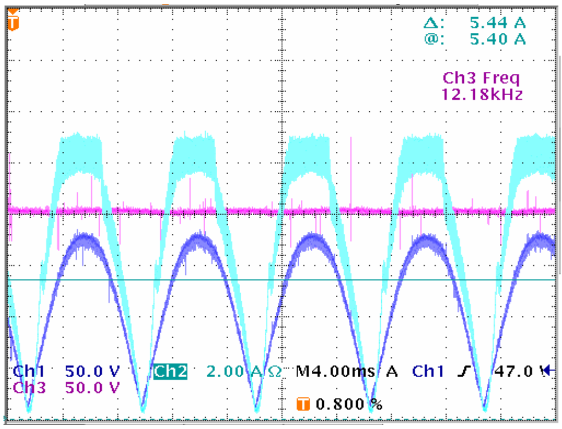

Figure 3. Active PFC Voltage and Current at 800 W loading

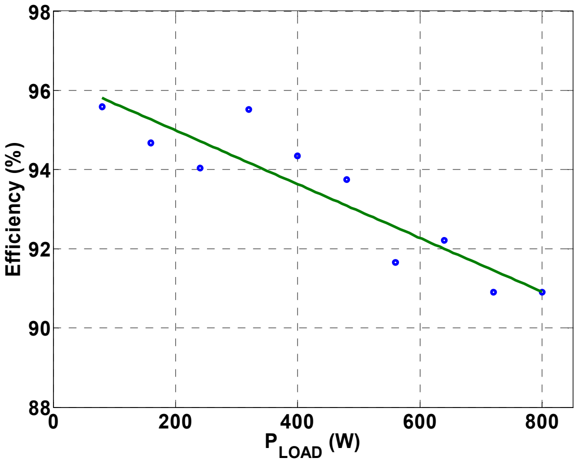

Figure 4. Active PFC Boost Circuit Efficiency

III. HEX-BRIDGE INVERTER

Cost was the major factor in the inverter design. To address this issue, the design focused on reducing the parts count in inverter through use of an integrated gate drive section. Instead of using six gate drive circuits, three of which need isolated supplies, and dead time circuitry, we used the IR21362. It is a low cost 3-phase bridge driver that has the three high side drivers utilizing flying capacitors and integrated dead time. The single IC solution not only lowers cost but it also increases the system's mean time between failures (MTBF).

The hex bridge was designed with 400V, 17 A MOSFETs (FQP17N40). The inverter and power supply board is shown in Figure 5. The inverter is modulated using selective harmonic elimination (SHE), discussed below. As a direct result of the lower switching frequency of SHE., minimal heat sinking is required for the MOSFETS and the inverter efficiency is increased compared to other PWM techniques. The efficiency at rated speed over a load range is presented in Figure 6.

IV. INDUCTION MOTOR DESIGN

The vast majority of the low cost induction machines on the market have been optimized for use in line-start applications. Constraints involving starting current and starting torque

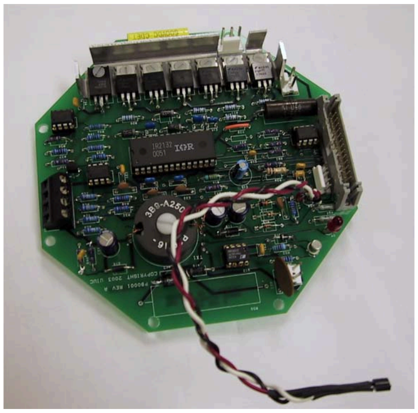

Figure 5. Inverter and Power Supply Board

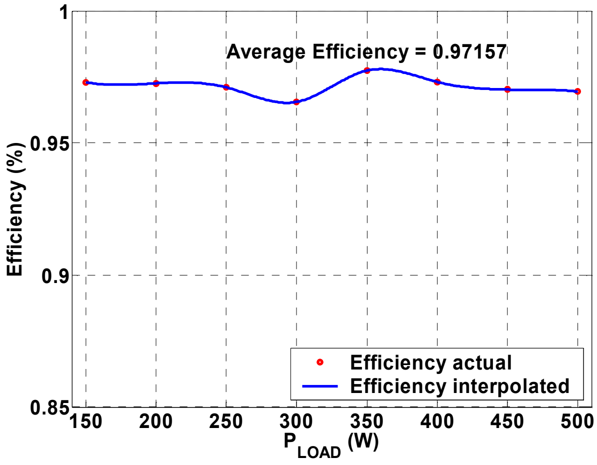

Figure 6. Inverter Efficiency at Rated Speed (1500 R.P.M.)

compromise the efficiency in the nominal operating range of these standard designs. Inverter fed induction machines designs do not require line-start considerations. This allows for higher efficiency in the low slip regime indicated in Figure 7, which is optimal since the inverter always operates the induction machine in the low slip regime. Additionally, line starts can be neglected due to the variable frequency nature of the power electronic inverter.

The induction machine was designed using Ansoft's RMXprt™. The design focused on the shape of the rotor slots, given a certain stator configuration using a Monte Carlo optimization approach [5]. Figure 8 shows the stator and rotor laminations. The large rotor slots decrease the rotor resistance and losses in the rotor. The rotor and stator assemblies are shown in Figure 9 and Figure 10 respectively. The motor efficiency was tested at a rated speed of 1500rpm and the efficiency results are shown in Figure 11. The motor operates with high efficiency across a broad range of torque values, which is required to meet specifications for this project. The results shown in Figure 11 are at rated flux and do not reflect flux optimization at lower loads.

V. HARMONIC ELIMINATION

Selective harmonic elimination (SHE) was first demonstrated in the early 1970's [6]. Presumably due to cost considerations, SHE has not been widely adopted in applications, despite benefits compared to PWM. Recent low cost fixed-point DSPs or microcontrollers allow for cost competitive implementation of SHE in high volume applications. This application utilizes a technique similar to traditional S.H.E where the switching angles are defined by the solution of

$$f_n(\delta) = \frac{4}{\pi}\left(\frac{\sin\left(\frac{n\pi}{2}\right)}{n} + \sum_{i=1}^{\substack{\#\text{of controlled} \\ \text{harmonics}}} 2(-1)^{i} \frac{\sin\left(\frac{n\pi}{2}\right)}{n} \cos\left(\frac{n\delta_i}{2}\right) \right) - m_n = 0 \qquad (1.1)$$

where n is the number of the harmonic being controlled and $\delta_i/2$ is the switching angle in radians of the i^{th} quasi-square wave. In previously proposed techniques, the state of the waveform at the zero crossings of the fundamental frequency is inconsistent while varying the number of harmonics eliminated [7]. The technique used guarantees the waveform state at zero crossings independent of the number of harmonics controlled

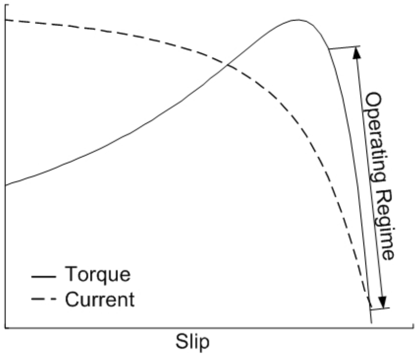

Figure 7. Nominal operating regime of an induction machine

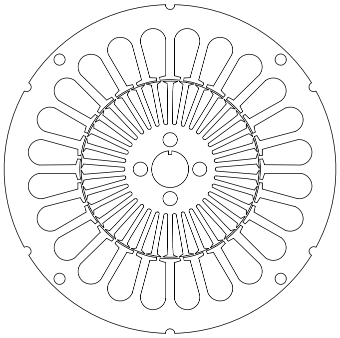

Figure 8. Rotor and Stator Laminations

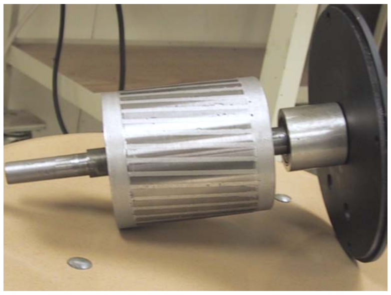

Figure 9. Rotor Assembly

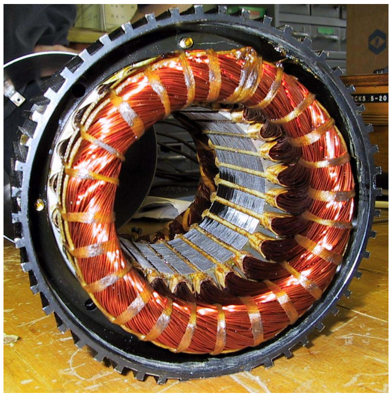

Figure 10. Stator Assembly

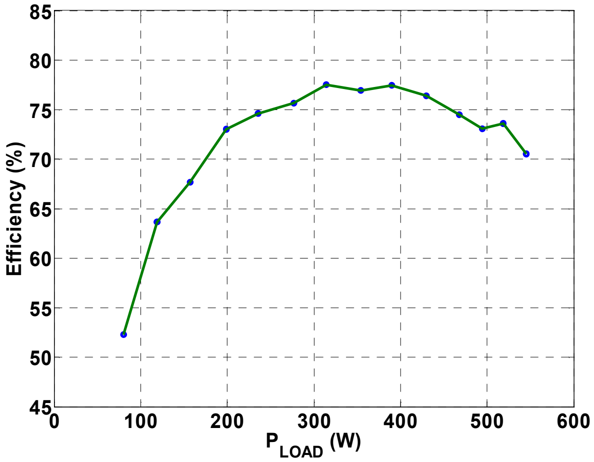

Figure 11. Induction Motor Efficiency at 1500 R.P.M.

provided that the harmonics controlled are the first n-1odd harmonics above the fundamental (i.e. 3-31 for $n = 16$).

The switching frequency, f_{switch}, of this harmonic elimination technique scales with the number of harmonics controlled, n, and the desired output frequency, $f_{fundamental}$, and is expressed as

$$f_{switch} = (2n+1) f_{fundamental} \tag{1.2}$$

The resulting switching frequency is significantly lower than PWM or vector based control algorithms particularly during low speed operation. Furthermore, it gives direct control over the harmonic content in the output voltage and current waveforms. The 3rd, 5th, 7th ….31st harmonics were controlled for this drive system. The switching function and its harmonic content are presented in Figure 12. The switching waveforms were tested at 60 Hz (although similar results hold for all fundamental frequencies of interest) with the hex-bridge inverter and an induction motor and are shown in Figure 13.

VI. SYSTEM POWER SUPPLY

The iDRIVE utilizes a flyback converter based on Power Integration's TNY267 to provide isolated supply power to the control circuitry. The TNY267 operates over a wide range of bus voltages as low as 50 V allowing the flyback converter to power up directly off of the classical input rectifier until the boost PFC raises the bus to 200V_{dc}. The tiny switch uses a hysteretic based control to regulate the output voltages on the secondary [8]. The TNY267 was chosen due to the low cost and reduced parts count compared to a complete standard flyback converter.

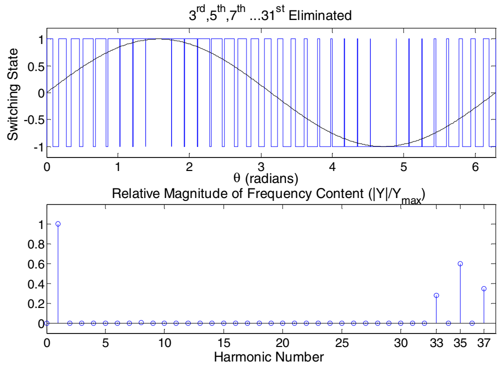

Figure 12. Switching Function and Harmonic Content

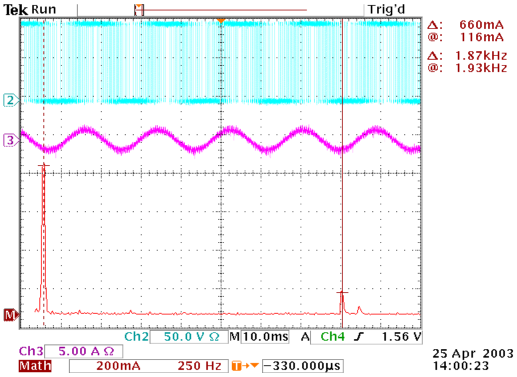

Figure 13. Motor Line to Line Voltage, Phase Current, and Current's Harmonic Content

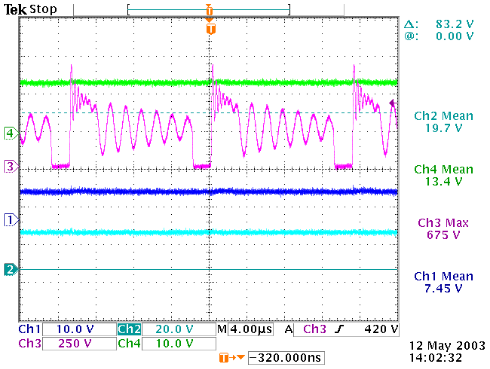

Figure 14. Flyback output voltages (19V, 13V, 7V) and power MOSFET drain source voltage

The flyback converter was designed with three secondary outputs, 19V_{dc}, 13V_{dc}, and 7V_{dc} with the 7V_{dc} supply regulated by the TNY267. 16V_{dc} and 5V_{dc} linear regulators stepped down the 19V_{dc} and 7V_{dc}, respectively, to guarantee stable supplies to the PFC IC, the Hex-bridge gate drive, and the DSP. The output voltages and the drain to source voltage of the power MOSFET in the TNY267 are shown in Figure 14.

VII. COST AND LIFETIME ANALYSIS

The design specifications require iDRIVE to have a manufacturing cost of $40 per unit in a million quantities. Initial cost analyses were performed based on production levels of 10,000 units with publicly available firm price quotes and are presented in Table 1. The per unit million quantity cost was estimated based upon the 10,000 unit production cost with additional cost savings based on integrated components (e.g. ASIC-based control circuitry).

The iDRIVE was designed to optimize manufacturability and reliability through low subsystem part counts and component re-usage. Reliability was estimated via MTBF as calculated per MIL-HDBK-217 for each sub-system as well as the complete system and is presented in . The expected system lifetime of 15.23 exceeds the desired lifetime of 10 years.

Table 1. Production Cost

Subsystem	10,000 Unit	Million Unit
PFC	$31.57	$12.32
Inverter	$11.18	$6.84
Flyback	$4.33	$1.54
Control	$24.95	$3.50
Motor	$24.56	$10.17
Misc.	$7.19	$3.39
Total	$103.77	$37.76

Table 2. Failure Rate and MTBF

Subsystem	**MTBF [Years]**
Support ICs	4563.61
Flyback	53.02
Inverter and Control	62.04
PFC	48.53
Total	15.23

VIII. SYSTEM INTEGRATION AND TESTING

In order to create a fully integrated motor and drive package, the power electronics were mounted at the end of the motor. This mounting allows for the motor's fan to provide active cooling for the power electronics. The packaging also provides minimal effort to set up the iDRIVE with only an input for speed control and an outlet for an IEC320 plug. The complete iDRIVE system is shown in Figure 15. Efficiency results for the integrated drive system are shown in Figure 16. These results were obtained with a constant V/Hz drive strategy without any form of flux weakening at light loads.

IX. CONCLUSIONS

The project met several of the target design goals including the power factor requirements, inrush currents, cost (estimated), and lifetime. The overall system performance of the iDRIVE fell short of the target efficiency marks as indicated in Figure 16. The primary difficulty was lower motor efficiencies than predicted from original design coupled with difficulties implementing a successful open loop flux weakening algorithm at light loads.

In addition to the actual hardware produced, the 2003 Future Energy Challenge had significant educational impact at the University of Illinois. Development of the drive was completed by 10 undergraduate students and 2 graduate students in conjunction with a semester course offering. Students were exposed to a variety of leadership and organizational challenges beyond what traditional courses require. Additionally, students gained practical experience in PCB design and system engineering. Many continued in power electronics related occupations or graduate school.

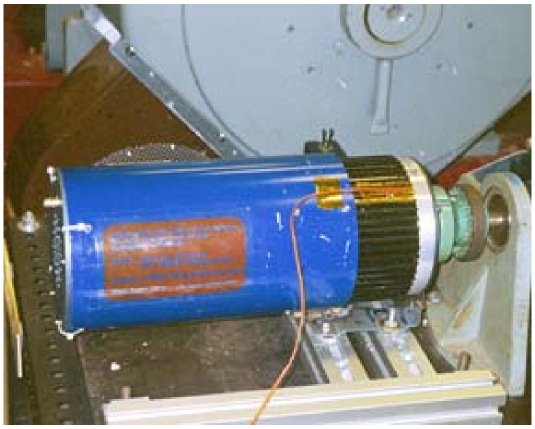

Figure 15. The iDRIVE

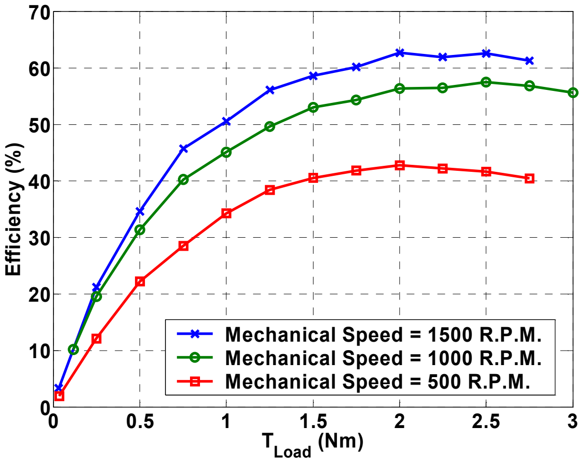

Figure 16. Efficiency at Various Operating Speeds for Complete System

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